REMARKS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks. In response to the Examiner's Action mailed June 20, 2001, the Applicants have amended Claims 1,12 and 24 and canceled Claims 2 and 14. In response to the present action, the Applications have amended Claims 1, 12 and 24. Supporting language may be found on Page 15, Lines 15-17 of the Specification. Accordingly, Claims 1, 4-12 and 15-24 are currently pending in the application.

I. Rejection of Claims 1, 5-6, 12, 16-17 and 24 under 35 U.S.C. §102

The Examiner has rejected Claims 1, 5-6, 12, 16-17 and 24 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,591,671 to Kim *et al.* ("Kim"). The Applicants respectfully disagree. For example, Kim does not disclose removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate. Rather, in order to prevent oxidation of his easily oxidizable refractory metal 28, ohmic contact layer 26 and barrier layer 27, the metal substance laminated on insulating layer 24 is etched-back, thereby leaving the metal substance only in the contact hole. (Column 5, Lines 24-66). The Applicants maintain that one of ordinary skill in the art would understand that etch-back entails etching below the surface of the substrate, as shown in Kim's FIGURE 4A. As such Kim fails to teach all elements of the claimed invention, and therefore does not anticipate Claims 1, 12 or 24, or their dependent Claims 5-6 and

16-17. For these reasons, the Applicants traverses the Examiner's rejection of Claims 1, 5-6, 12, 16-17 and 24 under 35 U.S.C. §102(b), and respectfully requests the Examiner withdraw the rejection.

II. Rejection of Claims 4, 8-11, 15 and 18-23 under 35 U.S.C. §103

The Examiner has rejected Claims 4, 8-10, 15, 19-21, and 23 under 35 U.S.C. §103(a) as being unpatentable over Kim. Claims 11 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kim in view of admitted prior art and U.S. Patent 5,913,141 to Bothra ("Bothra"). Claim is rejected under 35 U.S.C. §103(a) as being unpatentable over Kim in view U.S. Patent 5,985,751 to Koyama ("Koyama"). The Applicants respectfully maintain that the claimed invention is not obvious in view of the foregoing references, and that these references fail to establish a *prima facie* case of obviousness.

For example, nothing in Kim suggests that on removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate. To the contrary, Kim states that the metal is etched back such that the metal is only in the contact hole. (Column 5, Lines 64-65). Moreover, FIGURE 4B shows that the metal 28 is etched back below the level of the substrate so as to accommodate the deposit of cap layer 34 on the resultant structure prior to heating. (Column 5, Line 66 to Column 6, Line 2), which is also contrary to the presently claimed invention.

Neither Bothra nor Koyama cure the deficit teachings of Kim. For example, Bothra's CMP operation etches his aluminum layer 140 within the via holes (Column 6, Lines 53-55) and in one embodiment, enables the formation of a recess gap 145 (Column 7, Lines 4-7; FIGURE 6). Likewise Koyama's barrier metal layer of tungsten 17 is etched back and removed from the

insulating layer 20 to leave a plug 18 inside of the aperture portion 16. (Column 6, Lines 55-60; FIGURE 4A).

In summary, the combined teachings of Kim, the admitted prior art, Botha or Koyama do not teach or suggest all elements of the present invention and therefore fail to establish a *prima facie* case of obviousness with respect to independent Claims 1, 12 and 24 and there respective dependent Claims 4, 8-10, 15, 19-21, and 23. In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 4, 8-10, 15, 19-21, and 23 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

III. Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1, 4-12 and 15-24.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.

David H. Hitt
Registration No. 33,182

Dated: [illegible]

P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800
Email: dhitt@abstractassets.com

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1. (Three Times Amended) A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

(2) Kindly amend Claim 12 as follows:

12. (Three Times Amended) A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing by physical vapor deposition a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

(3) Kindly amend Claim 24 as follows:

24. (Twice Amended) A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate, wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate to form a contact plug within said contact opening, said plug extending to an uppermost surface of said substrate; and

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.